Single-Event Transient Response of InGaAs MOSFETs

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***Abstract*—The single-event-transient response of InGaAs MOSFETs exposed to heavy-ion and laser irradiations is investigated. The large barrier between the gate oxide and semiconductor regions effectively suppresses the gate transients compared with other types of III-V FETs. After the initial radiation-induced pulse, electrons and holes flood into the channel region at short time. The electrons are collected efficiently at the drain. The slower moving holes accumulate in the channel and source access region and modulate the source-channel barrier, which provides a pathway for transient source-to-drain current lasting for a few nanoseconds. The peak drain transient current reaches its maximum when the gate bias is near threshold and decreases considerably toward inversion and slightly toward depletion and accumulation. Two-dimensional TCAD simulations are used to understand the charge collection mechanisms.**

***Index Terms*—MOSFETs, quantum wells, single-event transient, technology computer-aided design (TCAD), two-photon absorption (TPA).**

I. Introduction

As silicon CMOS scaling reaches its limits, devices with III-V channels are promising candidates for future logic applications due to high electron velocity [1]. The low-power, high-speed nature of III-V MOSFETs represents an incentive for their use in space applications. Extensive research has been reported for III-V semiconductor single-event effects (SEE) [2]–[10], but most of that work focused on MESFET/HEMT devices rather than III-V MOSFET devices.

In this paper, we evaluate the charge collection in InGaAs MOSFETs. They are different from most III-V FETs in two important ways. First, they have an oxide layer, which can effectively prevent gate transients. In contrast, for GaAs MESFETs [4], AlSb/InAs HEMTs [6], and InAlAs/InGaAs HEMTs [8], gate transients are observed. Gate transients are also observed in AlGaN/GaN MOS-HEMTs with HfO_2 gate dielectric, which have a small barrier for holes to move into the gate, but not for devices with Al_2O_3 dielectrics, which have a larger barrier to hole motion [2]. In InGaAs MOSFETs, large barriers exist for both types of carriers, so the gate transients are largely suppressed.

The second difference is the source-channel barrier modulation observed in InGaAs MOSFETs. For many types of III-V devices that have been examined previously, single-event-induced source-channel barrier lowering occurs because of hole accumulation under the active layer. For example, for GaAs MESFETs [4], the holes that accumulate in the substrate beneath the channel tend to establish a transient conduction channel and create a pathway between the source and drain. However, for the devices investigated in this paper, the excess holes tend to accumulate in the channel layer, instead of beneath it, because of the deep type-I quantum well of these structures.

In this paper, we present the single-event transient response of InGaAs MOSFETs exposed to broadbeam heavy-ion irradiation and laser irradiation. The gate bias dependence of the charge-collection process is investigated. Two-dimensional technology computer-aided design (2-D TCAD) simulations are used to understand the charge collection mechanisms.

II. Device Description

The device under test (DUT) is a self-aligned InGaAs quantum-well MOSFET. Detailed device information is described in [11]. Fig. 1 shows the schematic cross section of the device (not drawn to scale). A 0.4 μm $In_{0.52}Al_{0.48}As$ buffer layer is grown on a 600 μm semi-insulating InP substrate. An 8 nm high-mobility $In_{0.7}Ga_{0.3}As$ surface channel enhances the device conductance. A HfO_2 gate dielectric sits directly on top of the channel. The inverted Si delta doping in the buffer layer is used to reduce source/drain access resistance and increase the channel carrier density [12].

The band diagram cut through the gate vertically is shown in Fig. 2. For this band diagram, all the terminals of the device are biased at 0 V. The device has a type-I heterostructure, which means that both the electrons and holes are confined in the channel region. This has a significant impact on the charge collection mechanisms.

Manuscript received July 11, 2014; revised September 03, 2014; accepted October 22, 2014. Date of publication November 13, 2014; date of current version December 11, 2014. This work was supported by the Defense Threat Reduction Agency through its Basic Research program and by the Air Force Research Laboratory and the Air Force Office of Scientific Research through the Hi-REV program.

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Digital Object Identifier 10.1109/TNS.2014.2365437

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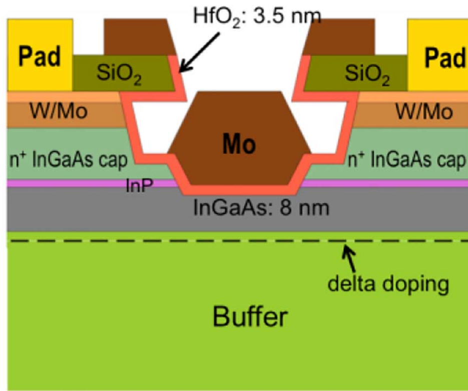

Fig. 1. Schematic cross section of devices under test (not drawn to scale).

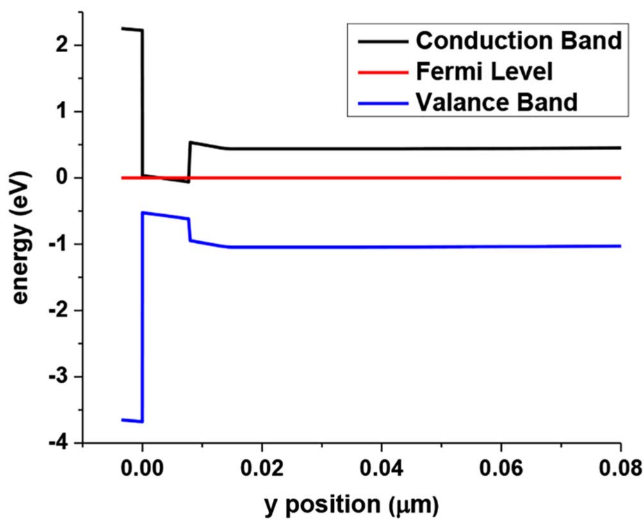

Fig. 2. Vertical band diagram of the device (all terminals are biased at 0 V for this band diagram).

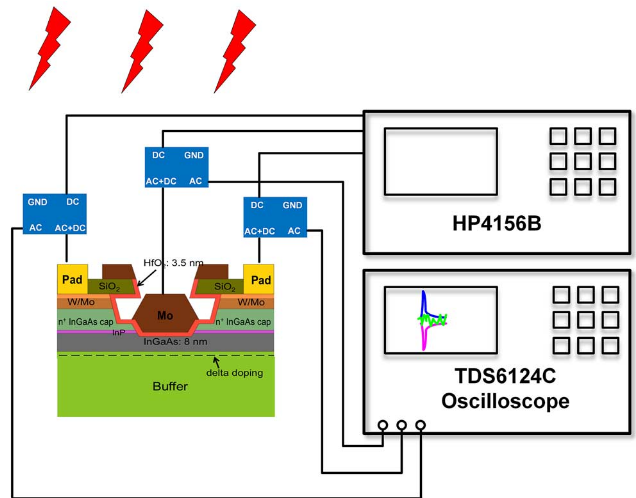

Fig. 3. Schematic diagram of the broadbeam heavy ion experiment setup.

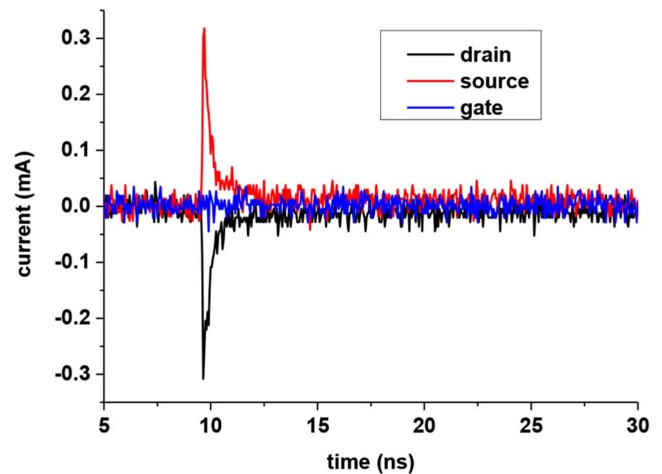

Fig. 4. Current transient of device 1 biased at $V_{GS} - V_{TH} = -0.2$ V, $V_{DS} = 0.5$ V with source grounded.

Three device layouts were tested. All devices have the same width, 10 μm. Device 1 has a gate length of 0.07 μm. Device 2 has a gate length of 0.2 μm, and device 3 has a gate length of 0.5 μm. For transient capture, all the devices are mounted in custom-milled metal packages with microstrip transmission lines and Precision 2.92 mm K connectors [2], [13].

III. Experimental Work

A. Broadbeam Ion Tests

For the broadbeam test, the devices were irradiated with 14.3 MeV oxygen ions in Vanderbilt's Pelletron electrostatic accelerator. Fig. 3 shows the schematic diagram of the experiment setup. From SRIM calculations, the ions have linear energy transfers (LETs) of 3.9 MeV-cm^2/mg, 4.1 MeV-cm^2/mg, and 4.2 MeV-cm^2/mg, respectively, in $In_{0.7}Ga_{0.3}As$, $In_{0.52}Al_{0.48}As$, and InP. The corresponding ion ranges are 6.9 μm, 7.4 μm, and 8.5 μm. Considering that the channel and buffer layer thicknesses are much smaller than the ion range, carriers are generated primarily in the InP substrate. In addition, the overlayer thickness is about 0.4 μm, which is much smaller than the ion range, about 3.6 μm, indicating very small energy loss in those materials.

The transients were captured using a Tektronix TDS6124C oscilloscope with 12 GHz front-end bandwidth and 20Gs/s sampling rate. Each oscilloscope channel has 50 Ω input impedance, which is used to convert the transient current to a measurable voltage. During these tests, the source and substrate were grounded, the drain bias was 0.5 V, and the gate bias was varied. A semiconductor parameter analyzer, HP 4156B, supplied the dc biases through Picosecond Model 5542 bias tees with 50 GHz bandwidth.

B. Broadbeam Results

A typical current transient is shown in Fig. 4. The source and drain transients have nearly the same magnitude but opposite polarity. The gate transients, if any, are indistinguishable from the background noise.

For the devices examined here, the $In_{0.7}Ga_{0.3}As/HfO_2$ conduction band offset is 2.2 eV and the valence band offset is 2.2 eV [14]. Since the barrier for both types of carriers in these

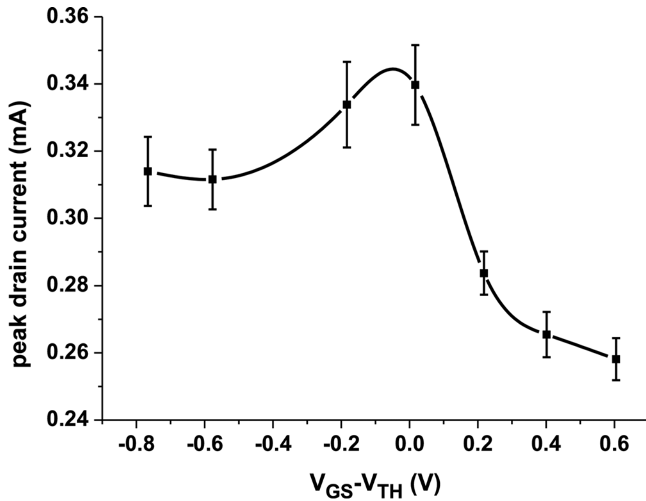

Fig. 5. Peak drain current versus gate bias of device 1 at $V_{DS} = 0.5$ V. The average flux is 1×10^8 particles/s • cm^{-2}.

devices is much larger than that for the AlGaN/GaN MOS HEMTs studied in [2], the gate oxide effectively suppresses the gate transients.

The shapes of the source and drain transients are similar to those reported in [3]. Following the strike, the source and drain currents increase sharply. After reaching the peak, they start to decay. The relaxation is related to processes with two distinct time constants. The fast collection is fairly rapid, with a time constant of approximately 300 ps or less. This fast collection is caused by the generated electrons that are collected by the drain. The longer time portion of the transient comes from a source-to-drain current pathway, which extends for about 3–5 ns. This results from the more slowly transporting holes. Following the ion strike, the generated electrons and holes under the channel layer flood into the channel region, because of the type-I band alignment. The electrons are rapidly swept toward the drain, but the slower holes (the electron mobility is around 50 times greater than the hole mobility) pile up in the channel and the source access region, lowering the source-channel barrier. As a result, electrons are injected from the source into the channel, and subsequently collected by the drain. This is illustrated in TCAD simulations in Section IV.

The gate-bias dependence of peak drain current was also investigated. In these tests, the drain bias voltage was 0.5 V, while the gate voltage was varied according to the pseudo-random sequence of 0 V, -0.4 V, 0.4 V, -0.8 V, 0.2 V, -1 V, -0.2 V, -0.6 V. This special sequence was selected to reduce any potential effects of device degradation on the measurement trends. Fig. 5 shows the peak drain current versus gate bias of one of the devices. The smooth curve is a spline fit to aid the eye. Other devices follow a similar trend. The error bars indicate the standard error of the mean. To keep the total fluence low, 30 transients were recorded for each bias point.

The peak drain current of the device decreases slightly in depletion and accumulation. Transients occur in inversion because the carrier density generated by radiation is higher than the carrier density induced by the applied gate bias. Moreover, the peak drain current decreases considerably in inversion. This is because channel inversion reduces the channel resistance, which becomes comparable with the source/drain access region resistance. As a result, the voltage dropped along the channel under the gate is less than the applied drain bias [5]. This reduces the horizontal electric field in the channel under the gate, and hence reduces the electron velocity. On the other hand, more electrons exist in the channel under more positive gate bias before the strike. For a given amount of carriers generated during the strike, most of the carriers are collected in the channel because of the type-I heterostructure, irrespective of the gate bias. Thus, the post-strike electron densities are almost the same under different gate biases. Consequently, the excess electron density, the absolute difference between post-strike electron density and prestrike electron density, decreases significantly in inversion. As a result, the peak drain current decreases considerably in inversion. This is illustrated by TCAD simulations in Section IV.

C. Laser Tests

The pulsed laser technique has been widely used for SEE testing [15]. High peak power femtosecond laser pulses at sub-bandgap optical wavelengths have been used as a viable alternative to conventional single-photon excitation to investigate the single event transient response of various devices based on two-photon absorption (TPA) [15]–[18]. Laser irradiations were performed at Vanderbilt University. The experimental setup is the same as Fig. 3 except that the laser pulse irradiation is from the backside. The detailed experimental setup is described in [17]. The laser wavelength is 1.26 μm and the nominal pulse width is approximately 150 fs. The DUT was fixed on an automated precision linear stage with a resolution of 0.1 μm. The stage jitter is about 0.2 μm. The optical pulses were focused onto the DUT using a 100× (NA 0.5) microscope objective with a charge generation spot size of approximately 1.2 μm in InGaAs.

The photon energy of the laser is 0.98 eV, which is greater than the bandgap of the channel material, $In_{0.7}Ga_{0.3}As$ (0.58 eV) [19]. For the laser experiment, the irradiance is approximately 2×10^8 W/cm^2. Considering that the linear absorption coefficient ($\sim 10^4$ cm^{-1}) is much larger than the TPA coefficient ($\sim$ 50 cm/GW [20]), the two-photon absorption in the channel region of these devices is much smaller than the single-photon absorption. This means that single-photon absorption dominates in the channel region. However, the photon energy is less than the band gap of the other materials, InP (1.35 eV) and $In_{0.52}Al_{0.48}As$ (1.45 eV) [19]. In these materials, TPA occurs, but the density of generated carriers is much smaller than that in the channel. Because both InP and $In_{0.52}Al_{0.48}$ As have a TPA coefficient of $\sim$ 30 cm/GW [21], the depth at which the beam intensity decays to half of the original value is ~ 3000 μm, which is larger than the buffer and substrate thickness. Considering the Gaussian beam profile, the high irradiance region extends $\sim$ 10 μm [16]. This is about a thousand times larger than the channel thickness, which compensates for the difference between the linear absorption coefficient in the channel and the TPA coefficient in the buffer and substrate. As a result, the buffer and substrate together have a comparable number of generated carriers with the channel layer.

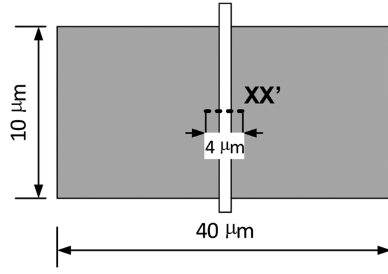

Fig. 6. Line scan (dashed black line XX') from -2 μm to 2 μm horizontally. The origin selected here is the center of the device.

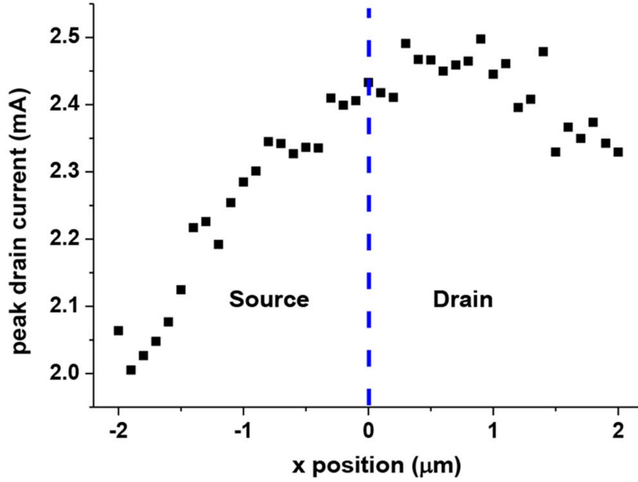

Fig. 7. Peak drain current of device 1 along the line scan XX' at bias $V_{GS} - V_{TH} = 0$ V, $V_{DS} = 0.5$ V. The laser pulse energy is around 0.55 pJ. The source side has a negative x coordinate, while the drain side is positive.

For the laser test, line scans were performed, so the position dependence of the induced transients could be evaluated. Fig. 6 shows the schematic diagram of the experiment used to obtain the line scan of the devices. The line scan XX' was from 2 μm to 2 μm horizontally. The center of the device is regarded as the origin.

D. Laser Results

Fig. 7 shows the peak drain current along the line scan XX' shown in Fig. 6. Other devices show similar behavior. The average laser pulse energy for each line scan is approximately 0.55 pJ. The drain side strike has a higher peak current compared with the source side strike. This is consistent with the applied bias between the drain and source contact, $V_{DS} = 0.5$ V. Consequently, the electric field on the drain side is larger than the source side. The carriers generated by the laser pulses move at a higher velocity in the drain side, which leads to larger peak current. Thus the drain side has a higher sensitivity to the irradiation.

The transients were investigated under different gate biases. Fig. 8 shows the peak drain current under different gate biases. Each data point is taken by averaging the drain peak current along a line scan XX', as shown in Fig. 6. The statistical standard error of the mean for each bias point is less than 5%. All the other devices follow a similar trend. The peak drain current reaches a maximum around the threshold voltage. Furthermore,

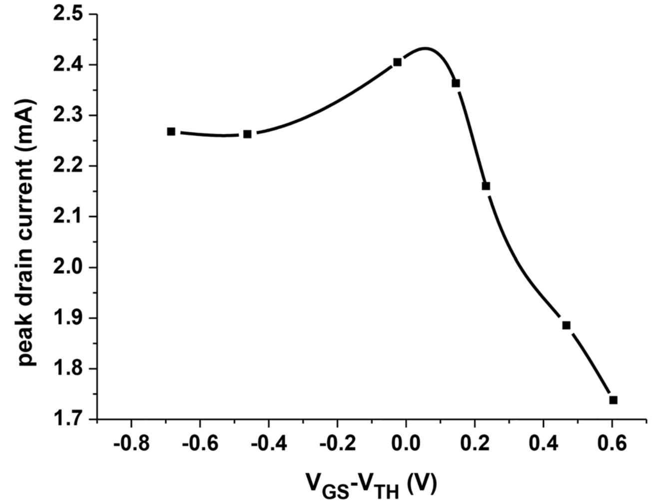

Fig. 8. Drain peak current versus gate bias at $V_{DS} = 0.5$ V (each data point is taken as the average of a line scan) of device 1. The small error bar is neglected.

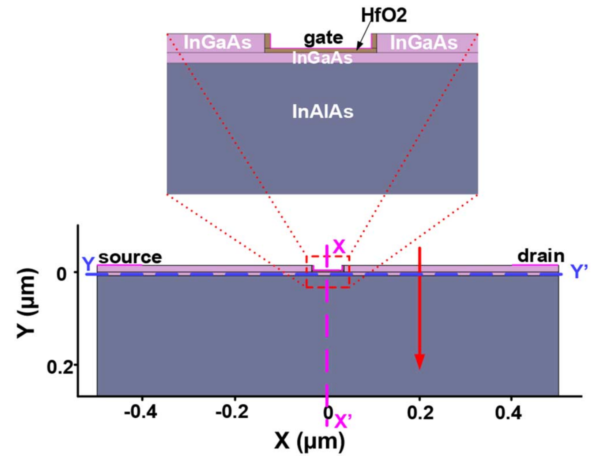

Fig. 9. Device model that is used in the 2-D TCAD simulation. Red arrow indicates the center of strike location. Synopsys Sentaurus TCAD tools are used here for simulation.

the current decreases considerably in inversion and decreases slightly in depletion and accumulation. This result is consistent with the broadbeam heavy ion data.

IV. TCAD Simulations

In this section, 2-D TCAD simulations are used to illustrate the mechanisms of charge collection in these devices. Fig. 9 shows the structure used for the TCAD simulations. The gate length is 70 nm, the same as device 1. The ion strikes are defined to be Gaussian both in time and space. The Gaussian heavy ion model has a characteristic width of 10 nm in space and 2 ps in time. The LET used to illustrate the mechanisms corresponds to charge deposition of 0.1 pC/μm, approximately the LET used in the broadbeam heavy ion experiment. The red arrow indicates the center of the strike location for the simulation (between the gate and drain), which is $x = 0.2$ μm. The time center of the strike is $t = 1.0$ ns.

Fig. 10 shows the hole density and the electric potential in the device at $t = 1.0$ ps (prestrike), 1.0 ns (center of strike), and 1.2 ns (post-strike), respectively. At the time of the strike,

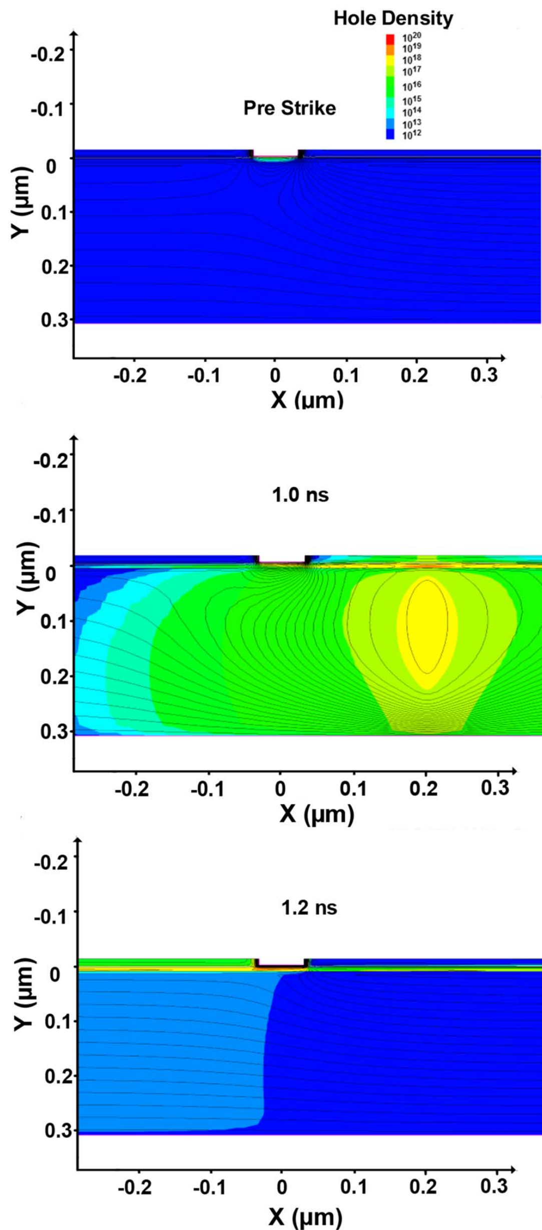

Fig. 10. Hole density and electrical potential plotted at 1.0 ps (prestrike), 1.0 ns, and 1.2 ns. The hole density is shown as color map and the electrical potential is shown as the equipotential line. The device is biased at $V_{GS}-V_{TH}=-0.2$ V, $V_{DS}=0.5$ V. Only the region around the channel is shown for clarity.

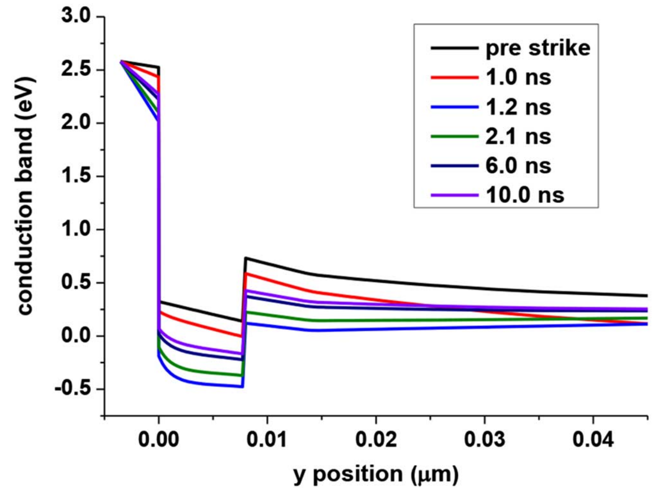

Fig. 11. Conduction band along the vertical cut XX', shown in Fig. 9, at different time. Only the portion around the channel is shown for clarity.

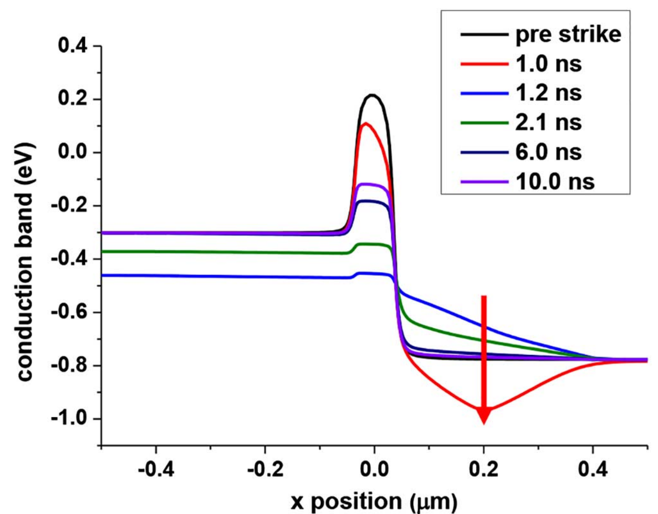

Fig. 12. Conduction band along the horizontal cut,YY', shown in Fig. 9, at different time. The bias condition is the same as shown in Fig. 10.

a large number of electron hole pairs are created around the strike location. As a result, the electric potential is strongly distorted compared with the prestrike condition ($t=1.0$ ps). At 1.2 ns, the potential in the thick buffer layer has almost recovered and the holes in the buffer are mostly collected, especially at the drain side. This confirms that the generated electrons and holes soon move into the channel layer because of the type-I heterostructure.

This behavior is further illustrated in Fig. 11 by the band diagram evolution in time along the vertical cut XX'. In the prestrike condition, there is an electric field produced by the gate bias, which keeps electrons from entering the quantum well. Just after the strike, at 1.2 ns, however, this electric field in the buffer is so small that both types of carriers can flow into the channel region.

After 1.2 ns, only the channel region is strongly perturbed as a large number of electrons and holes are collected there. The process of collecting these carriers lasts for a few nanoseconds as illustrated in Fig. 4. To understand this process, Fig. 12 shows the time evolution of the conduction band along the horizontal cut, YY'. At 1.0 ns, the electrostatic potential around the strike location is strongly distorted by the generated carriers. Soon after the strike, the conduction band recovers on the drain side at 1.2 ns. This confirms that the generated electrons are collected quickly by the drain. Following the strike, the source channel barrier is lowered from 0.52 eV to 0.03 eV at 1.2 ns as holes pile up in the channel layer right under the gate and source access region. The barrier keeping the electrons from being injected from the source to channel is quite small. The transistor turns ON and current flows between source and drain. As holes reach the source where they recombine, the electric potential recovers

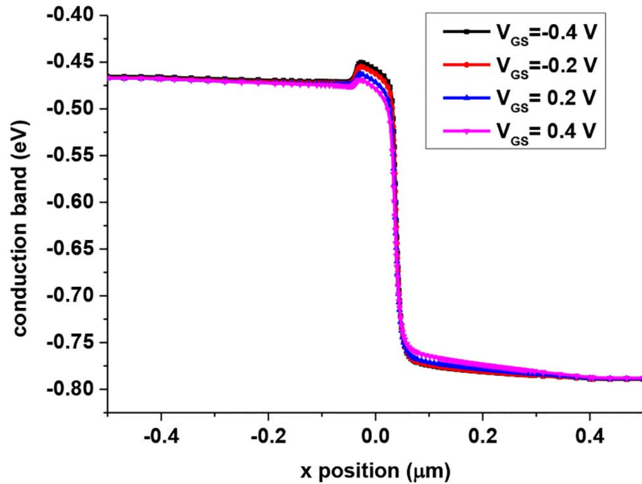

Fig. 13. Conduction band along the horizontal cut YY' in the channel layer under different gate biases at 1.2 ns (200 ps after the center of the strike).

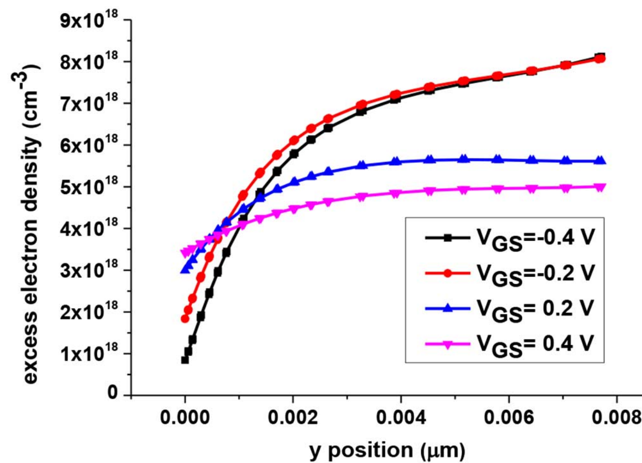

Fig. 14. Electron density along the vertical cut XX' under different gate biases at 1.2 ns (200 ps after the center of strike). For clarity, only electron density in the channel region is shown. $V_{TH} = -0.2$ V.

to the prestrike value. Eventually, the source channel barrier returns to 0.52 eV.

The gate bias dependence of the response is also simulated. Fig. 13 shows the conduction band along the horizontal cut YY' under different gate biases at 1.2 ns. The source channel barriers preventing carriers from being injected from the source are small under all gate biases. The potential drop along the channel region is reduced with increasing gate bias. This leads to a smaller horizontal electric field along the channel, which translates into smaller electron velocity at higher gate bias.

Fig. 14 presents the excess electron density, the absolute electron density difference between the post-strike and prestrike conditions, along the vertical cut XX' under different gate biases at 1.2 ns. As the gate bias increases, the excess electron density in the channel reaches a maximum for gate voltages near the threshold, and decreases slightly in depletion and considerably in inversion. Although there is a slight increase in the post-strike electron density with the gate bias, the increase with gate bias is small. This is because for a given amount of generated carriers, most of them will be collected in the channel layer, irrespective of the gate bias. The gate bias does not have a large effect on the post-strike electron density in the channel due to the electric potential distortion caused by the large number of carriers. As a result, the higher the prestrike electron density, the smaller the excess electron density will be. Thus, for gate biases in inversion, the reduced excess electron density and the reduced electron velocity cause a significant decrease in peak drain current. For gate biases in depletion and accumulation, the excess electron density is slightly smaller than the density in threshold, which causes a slight decrease of the peak drain current [5].

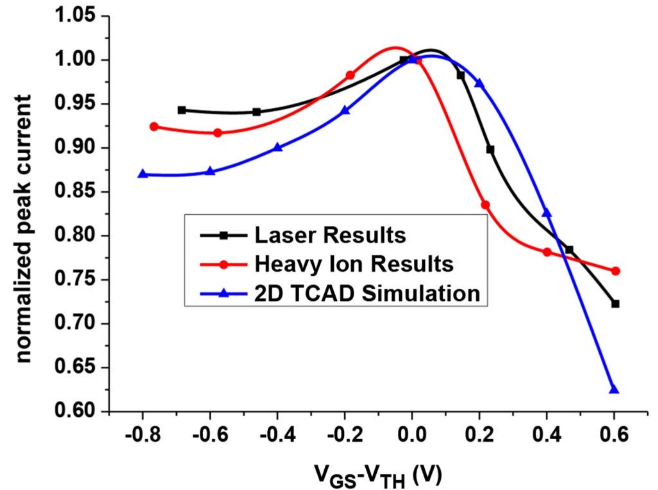

Fig. 15. Normalized peak drain current of heavy ion experiment, laser experiment, and 2-D TCAD simulation. The maximum peak drain currents are 2.4 mA, 0.34 mA, and 48 mA for laser, heavy ion, and TCAD simulation, respectively. The quantitative differences in peak current result from parasitic capacitance and inductance that exist in the experimental configuration that are not replicated in the simulations. But the trends in peak current are replicated well via simulation.

Fig. 15 shows the normalized peak drain currents for the heavy ion experiment, the laser experiment, and the 2-D TCAD simulations. Each set is normalized by its own maximum peak current, which occurs near $V_{GS} - V_{TH} = 0$ V. The TCAD simulations describe trends in the gate bias dependence of the peak drain current quite well, showing that the peak drain current decreases considerably in inversion and decreases slightly in depletion and accumulation.

V. Conclusions

The single-event-transient response of InGaAs MOSFETs is investigated through broadbeam heavy ion and laser irradiation. The large conduction band offset and valence band offset between the gate dielectric and semiconductor regions effectively suppress the gate transients. The deep type-I heterostructure strongly affects the charge collection process. The generated carriers are collected in the quantum well (channel layer). The slow holes pile up under the gate and the source access region, which reduces the source channel barrier height. More electrons are injected from the source to the drain, enhancing the collected charge. The peak drain current reaches a maximum near the threshold voltage and decreases considerably in inversion and

slightly in depletion and accumulation. These results, coupled with previous work, show that the charge collection in MOSFETs can vary strongly with channel technology and gate stack materials. Depending on the application and the opportunities for remediation, these transient responses may impose limitations on the use of some types of alternative-channel materials in space applications.

References

[1] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, Nov. 2011.

[2] I. K. Samsel, E. X. Zhang, N. C. Hooten, E. D. Funkhouser, W. G. Bennett, R. A. Reed, R. D. Schrimpf, M. W. McCurdy, D. M. Fleetwood, R. A. Weller, G. Vizkelethy, X. Sun, T. P. Ma, O. I. Saadat, and T. Palacios, "Charge collection mechanisms in AlGaN/GaN MOS high electron mobility transistors," *IEEE Trans. Nucl. Sci*, vol. 60, no. 6, pp. 4439–4445, Dec. 2013.

[3] D. McMorrow, J. B. Boos, A. R. Knudson, W. T. Lotshaw, D. Park, J. S. Melinger, B. R. Bennett, A. Torres, V. F. Cavrois, J. E. Sauvestre, C. D. Hose, and O. Flament, "Transient response of III-V field-effect transistors to heavy-ion irradiation," *IEEE Trans. Nucl. Sci*, vol. 51, no. 6, pp. 3324–3331, Dec. 2004.

[4] D. McMorrow, T. R. Weatherford, S. Buchner, A. R. Knudson, J. S. Melinger, L. H. Tran, and A. B. Campbell, III, "Single event phenomena in GaAs devices and circuits," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 628–644, Apr. 1996.

[5] S. DasGupta, D. McMorrow, R. A. Reed, R. D. Schrimpf, and J. B. Boos, "Gate bias dependence of single event charge collection in AlSb/InAs HEMTs," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 1856–1860, Aug. 2010.

[6] D. McMorrow, J. B. Boos, A. R. Knudson, S. Buchner, M. J. Yang, B. R. Bennett, and J. S. Melinger, "Charge-collection characteristics of low power ultrahigh speed, metamorphic AlSb/InAs high-electron mobility transistors (HEMTs)," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2662–2668, Dec. 2000.

[7] J. H. Warner, D. McMorrow, S. Buchner, J. B. Boos, N. Roche, P. Paillet, M. Gaillardin, E. Blackmore, M. Trinczek, V. Ramachandran, R. A. Reed, and R. D. Schrimpf, "Proton-induced transient charge collection in GaAs and InAlSb/InAs-based FETs," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2651–2659, Aug. 2013.

[8] D. McMorrow, A. R. Knudson, J. B. Boos, D. Park, and J. S. Melinger, "Ionization-induced carrier transport in InAlAs/InGaAs high electron mobility transistors," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 5, pp. 2857–2864, Oct. 2004.

[9] D. McMorrow, J. B. Boos, D. Park, S. Buchner, A. R. Knudson, and J. S. Melinger, "Charge collection dynamics of InP based high electron mobility transistors (HEMTs)," in *Proc. 6th Eur. Conf. Radiation Effects Components Syst*, 2001, pp. 132–137.

[10] V. Ramachandran, R. A. Reed, R. D. Schrimpf, D. McMorrow, J. B. Boos, M. P. King, E. X. Zhang, G. Vizkelethy, X. Shen, and S. T. Pantelides, "Single-event transient sensitivity of InAlSb/InAs/AlGaSb high electron mobility transistors," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2691–2696, Dec. 2012.

[11] J. Lin, X. Zhao, T. Yu, D. A. Antoniadis, and J. A. del Alamo, "A new self-aligned quantum-well MOSFET architecture fabricated by a scalable tight-pitch process," in *Proc. IEDM*, Mar. 2013, pp. 421–424.

[12] T. W. Kim, R. J. W. Hill, C. D. Young, D. Veksler, L. Morassi, S. Oktybrshky, J. Oh, C. Y. Kang, D.-H. Kim, J. A. del Alamo, C. Hobbs, P. D. Kirsch, and R. Jammy, "InAs quantum-well MOSFET (L_g = 100 nm) with record high g_m, f_T and f_{max}," in *Proc. Symp. VLSI Technol*, 2012, pp. 179–180.

[13] E. X. Zhang, D. M. Fleetwood, N. D. Pate, R. A. Reed, A. F. Witulski, and R. D. Schrimpf, "Time-domain reflectometry measurements of total-ionizing-dose degradation of nMOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4470–4475, Dec. 2013.

[14] M. F. Li, W. Cao, D. M. Huang, C. Shen, S. Q. Cheng, C. J. Yao, and H. Y. Yu, "Impact of gate dielectric geometry on the nanowire MOSFETs performance and scaling," *ECS Trans.*, vol. 35, pp. 383–401, 2011.

[15] J. S. Melinger, S. Buchner, D. McMorrow, W. J. Stapor, T. R. Weatherford, and A. B. Campbell, "Evaluation of the pulsed laser method for single event effects testing and fundamental studies," *IEEE, Trans. Nucl. Sci.*, vol. 41, no. 6, pp. 2574–2584, Dec. 1994.

[16] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, and R. L. Pease, "Subbandgap laser-induced single event effects: Carrier generation via two-photon absorption," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 3002–3008, Dec. 2002.

[17] N. C. Hooten, W. G. Bennett, L. D. Edmonds, J. A. Kozub, R. A. Reed, R. D. Schrimpf, and R. A. Weller, "The impact of depletion region potential modulation on ion-induced current transient response," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4150–4158, Dec. 2013.

[18] D. McMorrow, S. Buchner, W. T. Lotshaw, J. S. Melinger, M. Maher, and M. W. Savage, "Demonstration of single event effects induced by through wafer two photon absorption," *IEEE Trans. Nucl. Sci*, vol. 51, no. 6, pp. 3553–3557, Dec. 2004.

[19] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for III-V compound semiconductors and their alloys," *J. Appl. Phys*, vol. 89, pp. 5815–5875, Jun. 2001.

[20] S. Krishnamurthy, Z. G. Yu, L. P. Gonzalez, and S. Guha, "Accurate evaluation of nonlinear absorption coefficients in InAs, InSb, and HgCdTe alloys," *J. Appl. Phys*, vol. 101, no. 113104, 2007.

[21] D. Vignaud, J. F. Lampin, and F. Mollot, "Two-photon absorption in InP substrates in the $1.55\ \mu$m range," *Appl. Phys. Lett*, vol. 85, pp. 239–241, 2004.